

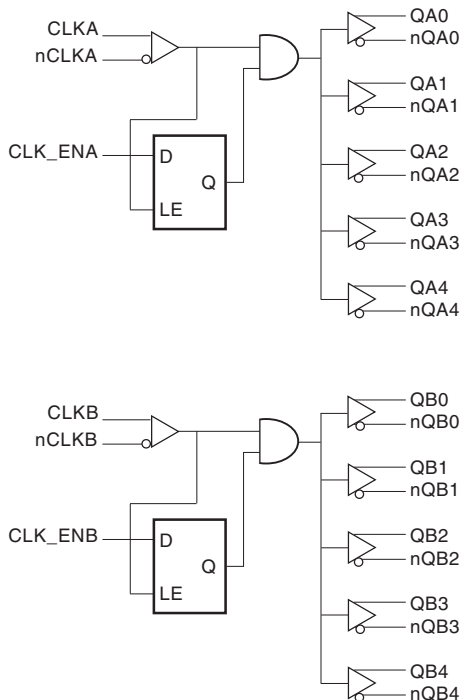
### GENERAL DESCRIPTION

The ICS85310I-31 is a low skew, high performance dual 1-to-5 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLKx, nCLKx pairs can accept most standard differential input levels. The ICS85310I-31 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS85310I-31 ideal for those clock distribution applications demanding well defined performance and repeatability.

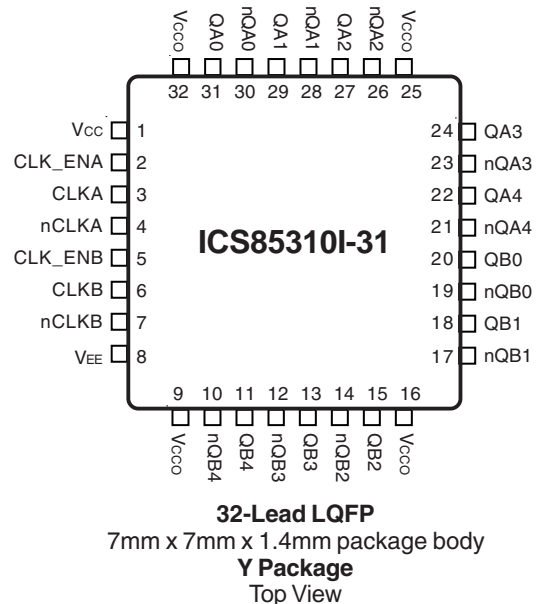
### FEATURES

- 2 differential 2.5V/3.3V LVPECL / ECL bank outputs
- 2 differential clock input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLKx input
- Output skew: 25ps (typical)
- Part-to-part skew: 270ps (typical)
- Propagation delay: 1.7ns (typical)
- Additive phase jitter, RMS: <0.13ps (typical)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to  $3.8V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -3.8V$  to  $-2.375V$
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

### BLOCK DIAGRAM



### PIN ASSIGNMENT





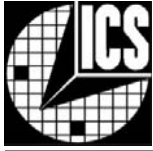
**TABLE 1. PIN DESCRIPTIONS**

| Number        | Name             | Type   |          | Description  |
|---------------|------------------|--------|----------|--|
| 1             | V <sub>CC</sub>  | Power  |          | Core supply pin.   |
| 2             | CLK_ENA          | Unused | Pullup   | Synchronizing clock enable. LVCMOS/LVTTL interface levels. |
| 3             | CLKA             | Input  | Pulldown | Non-inverting differential clock input.                    |
| 4             | nCLKA            | Input  | Pullup   | Inverting differential clock input.                        |
| 5             | CLK_ENB          | Unused | Pullup   | Synchronizing clock enable. LVCMOS/LVTTL interface levels. |
| 6             | CLKB             | Input  | Pulldown | Non-inverting differential clock input.                    |
| 7             | nCLKB            | Input  | Pullup   | Inverting differential clock input.                        |
| 8             | V <sub>EE</sub>  | Power  |          | Negative supply pin.                                       |
| 9, 16, 25, 32 | V <sub>CCO</sub> | Power  |          | Output supply pins.  |
| 10, 11        | nQB4, QB4        | Output |          | Differential output pair. LVPECL interface levels.         |
| 12, 13        | nQB3, QB3        | Output |          | Differential output pair. LVPECL interface levels.         |
| 14, 15        | nQB2, QB2        | Output |          | Differential output pair. LVPECL interface levels.         |
| 17, 18        | nQB1, QB1        | Output |          | Differential output pair. LVPECL interface levels.         |
| 19, 20        | nQB0, QB0        | Output |          | Differential output pair. LVPECL interface levels.         |
| 21, 22        | nQA4, QA4        | Output |          | Differential output pair. LVPECL interface levels.         |
| 23, 24        | nQA3, QA3        | Output |          | Differential output pair. LVPECL interface levels.         |
| 26, 27        | nQA2, QA2        | Output |          | Differential output pair. LVPECL interface levels.         |
| 28, 29        | nQA1, QA1        | Output |          | Differential output pair. LVPECL interface levels.         |
| 30, 31        | nQA0, QA0        | Output |          | Differential output pair. LVPECL interface levels.         |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

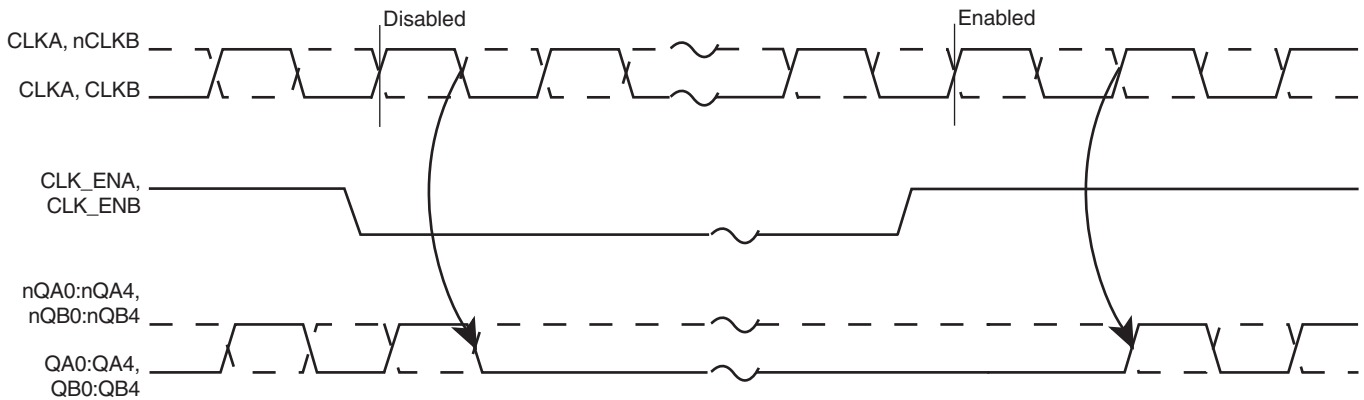


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

| Inputs               | Outputs          |                      |
|----------------------|------------------|----------------------|
|                      | QA0:QA4, QB0:QB4 | nQA0:nQA4, nQB0:nQB4 |
| CLK_ENA, CLK_ENB = 0 | Disabled; LOW    | Disabled; HIGH       |
| CLK_ENA, CLK_ENB = 1 | Enabled          | Enabled              |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLKA, nCLKA and CLKB, nCLKB inputs as described in Table 3B.



**FIGURE 1. CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

| Inputs         |                | Outputs          |                      | Input to Output Mode         | Polarity      |
|----------------|----------------|------------------|----------------------|------------------------------|---------------|
| CLKA or CLKB   | nCLKA or nCLKB | QA0:QA4, QB0:QB4 | nQA0:nQA4, nQB0:nQB4 |                              |               |
| 0              | 1              | LOW              | HIGH                 | Differential to Differential | Non Inverting |
| 1              | 0              | HIGH             | LOW                  | Differential to Differential | Non Inverting |
| 0              | Biased; NOTE 1 | LOW              | HIGH                 | Single Ended to Differential | Non Inverting |
| 1              | Biased; NOTE 1 | HIGH             | LOW                  | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0              | HIGH             | LOW                  | Single Ended to Differential | Inverting     |
| Biased; NOTE 1 | 1              | LOW              | HIGH                 | Single Ended to Differential | Inverting     |

NOTE 1: Please refer to the Application Information "Wiring The Differential Input To Accept Single Ended Levels".



### ABSOLUTE MAXIMUM RATINGS

|  |                          |
|--|--------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                     |
| Inputs, $V_i$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_o$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC}, V_{CCO} = 2.375V$  to  $3.8V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$  | Core Supply Voltage   |                 | 2.375   | 3.3     | 3.8     | V     |
| $V_{CCO}$ | Output Supply Voltage |                 | 2.375   | 3.3     | 3.8     | V     |
| $I_{EE}$  | Power Supply Current  |                 |         |         | 120     | mA    |

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC}, V_{CCO} = 2.375V$  to  $3.8V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter          | Test Conditions                                  | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|--|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage | CLK_ENA, CLK_ENB                                 | 2       |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  | CLK_ENA, CLK_ENB                                 | -0.3    |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | CLK_ENA, CLK_ENB<br>$V_{CC} = V_{IN} = 3.8V$     |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK_ENA, CLK_ENB<br>$V_{CC} = 3.8V, V_{IN} = 0V$ | -150    |         |                | $\mu A$ |

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC}, V_{CCO} = 2.375V$  to  $3.8V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter                            | Test Conditions | Minimum                      | Typical | Maximum         | Units   |
|-----------|--------------------------------------|-----------------|------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                   | CLKA, CLKB      | $V_{CC} = V_{IN} = 3.8V$     |         | 150             | $\mu A$ |
|           |                                      | nCLKA, nCLKB    | $V_{CC} = V_{IN} = 3.8V$     |         | 5               | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | CLKA, CLKB      | $V_{CC} = 3.8V, V_{IN} = 0V$ | -5      |                 | $\mu A$ |
|           |                                      | nCLKA, nCLKB    | $V_{CC} = 3.8V, V_{IN} = 0V$ | -150    |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage           |                 | 0.15                         |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                 | $V_{EE} + 0.5$               |         | $V_{CC} - 0.85$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLKA, nCLKA and CLKB, nCLKB is  $V_{CC} + 0.3V$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC}, V_{CCO} = 2.375V$  to  $3.8V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 1.0$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6             |         | 1.0             | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC}, V_{CCO} = 2.375V$  to  $3.8V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

| Symbol    | Parameter  | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--|-----------------|---------|---------|---------|-------|
| $f_{MAX}$ | Output Frequency   |                 |         |         | 700     | MHz   |
| $t_{PD}$  | Propagation Delay; NOTE 1  | $f \leq 500MHz$ |         | 1.7     | 2.2     | ns    |
| $tsk(o)$  | Output Skew; NOTE 2, 4   |                 |         | 25      | 50      | ps    |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 3, 4   |                 |         | 270     | 550     | ps    |
| $f_{jit}$ | Buffer Additive Phase Jitter, RMS;<br>refer to Additive Phase Jitter Section |                 |         | <0.13   |         | ps    |
| $t_R$     | Output Rise Time   | 20% to 80%      | 200     |         | 700     | ps    |
| $t_F$     | Output Fall Time   | 20% to 80%      | 200     |         | 700     | ps    |
| odc       | Output Duty Cycle  |                 | 47      |         | 53      | %     |

All parameters measured at 500MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

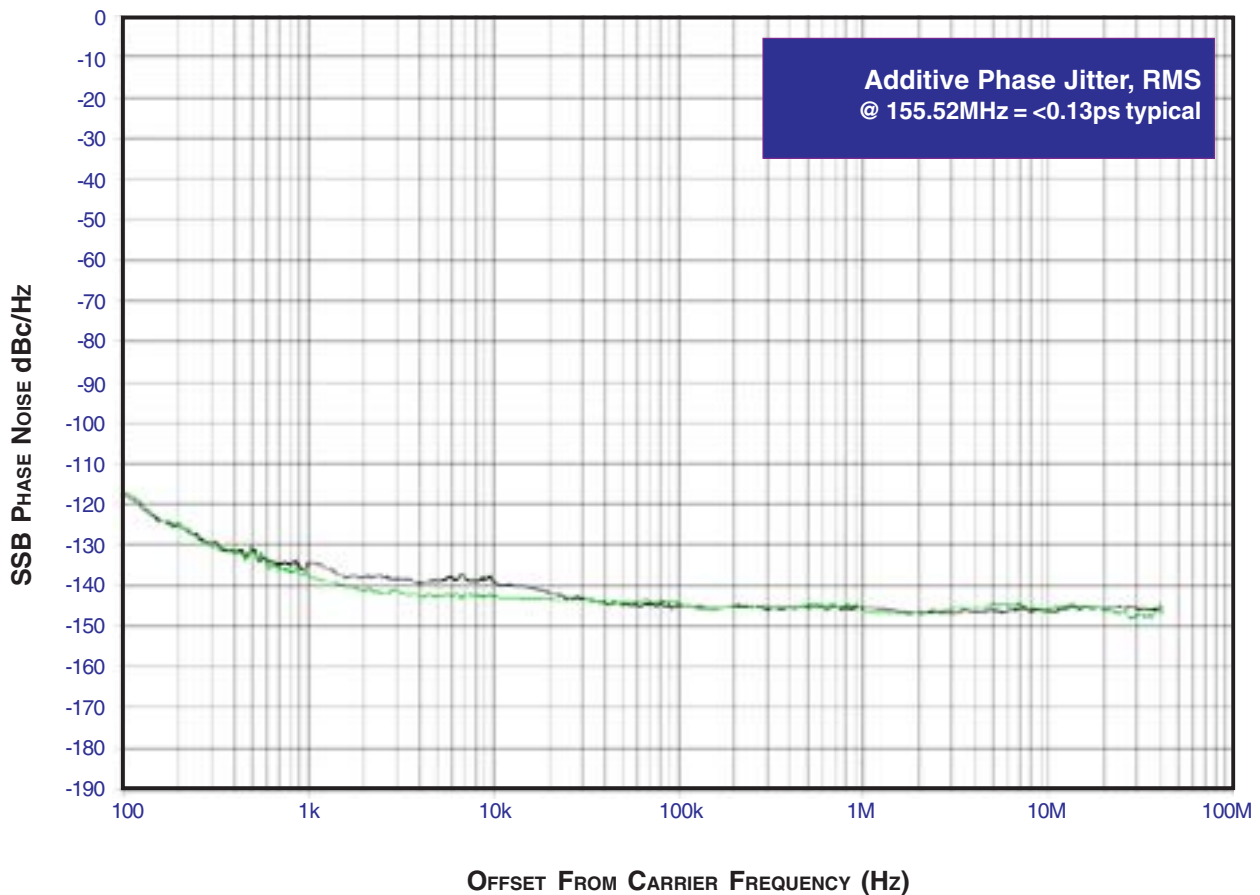
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



### ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in

the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

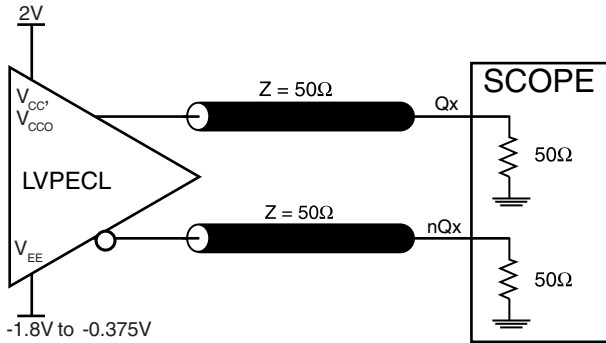


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The de-

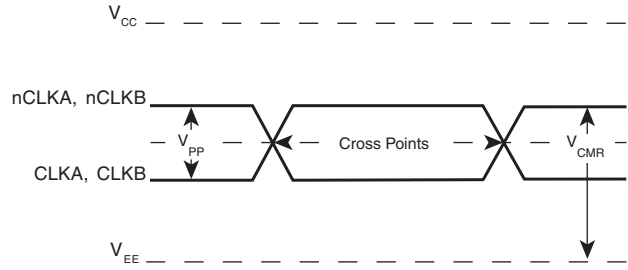
vice meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.



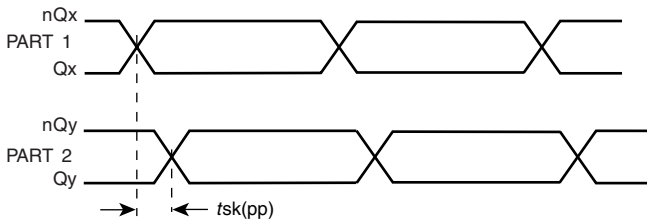
## PARAMETER MEASUREMENT INFORMATION



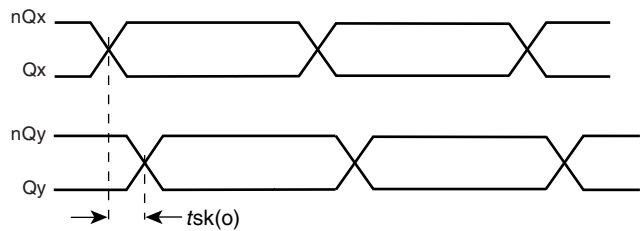
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



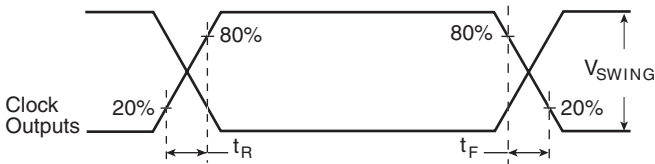
**DIFFERENTIAL INPUT LEVEL**



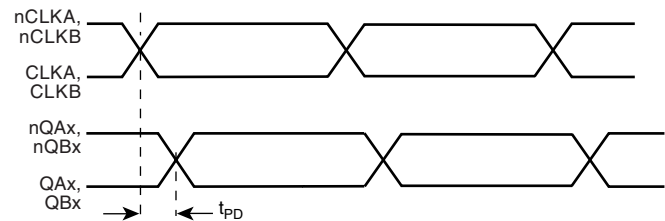
**PART-TO-PART SKEW**



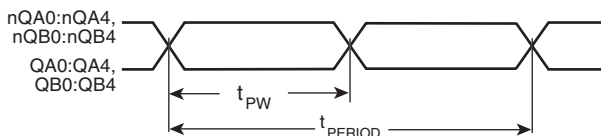
**OUTPUT SKEW**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

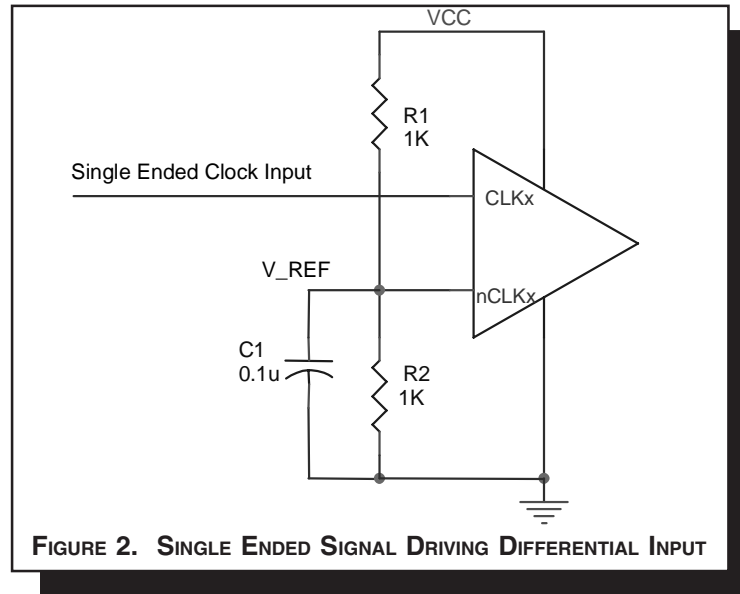


## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

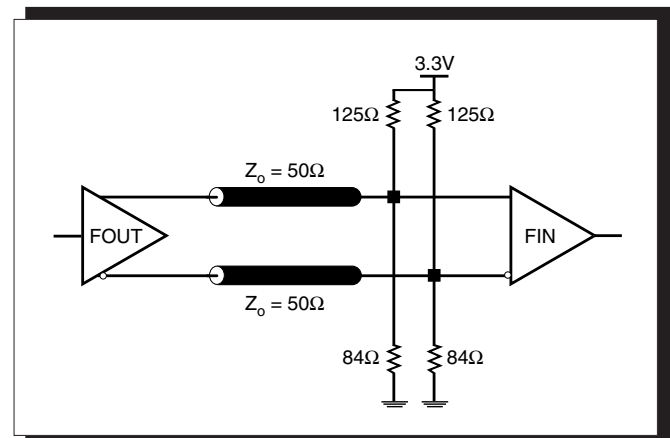
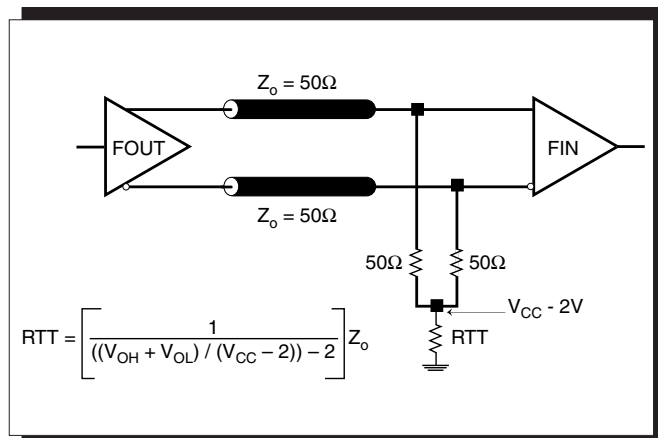


### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.







### TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to

ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

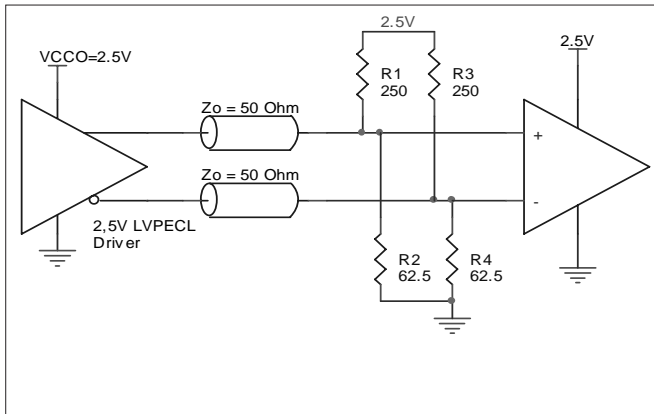


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

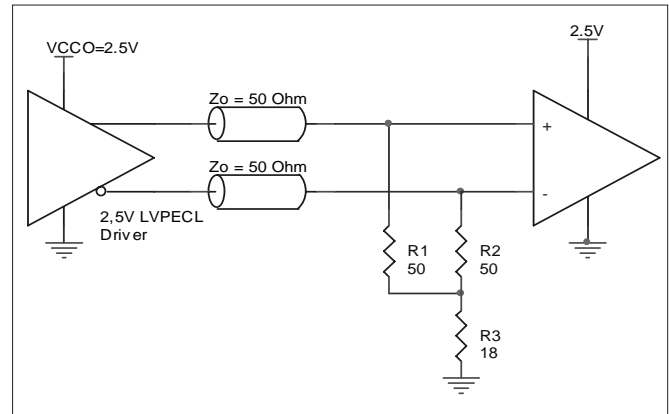


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

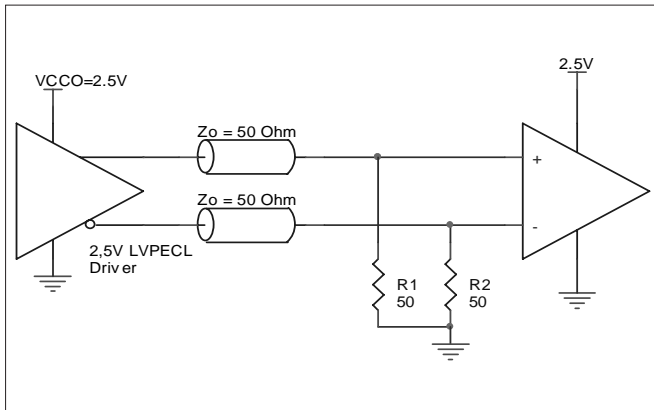


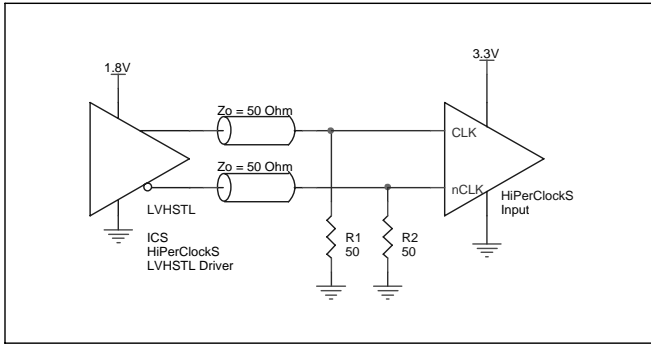
FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE



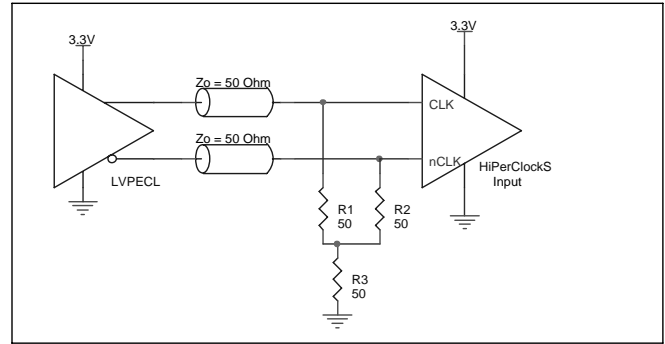
#### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 5A to 5E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

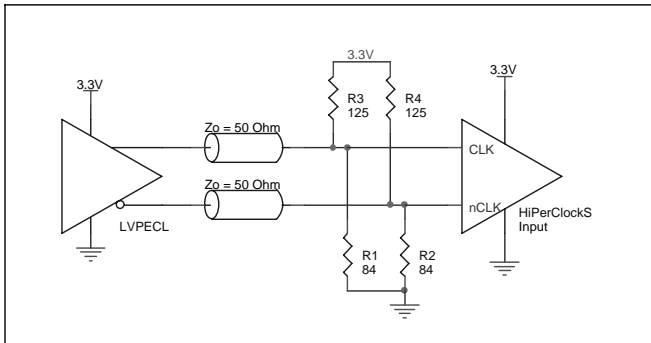
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



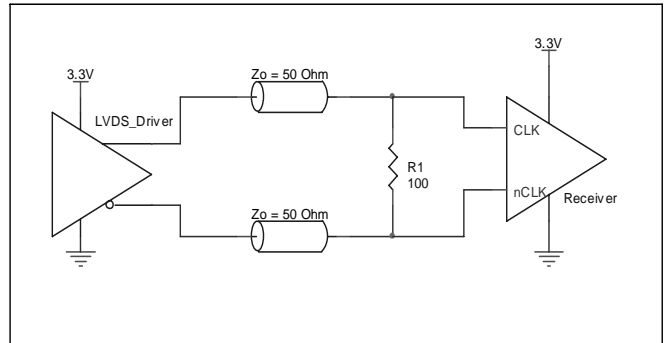
**FIGURE 5A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



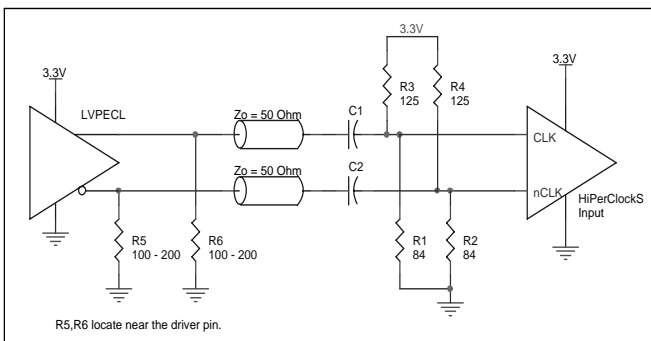
**FIGURE 5B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



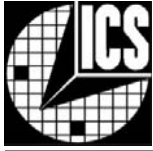
**FIGURE 5C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 5D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**FIGURE 5E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85310I-31. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS85310I-31 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.8V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.8V * 120mA = 456mW$
- Power (outputs)<sub>MAX</sub> = **30.94mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $10 * 30.94mW = 309.4mW$

**Total Power<sub>MAX</sub>** (3.8V, with all outputs switching) =  $456mW + 309.4mW = 765.4mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.765W * 42.1^\circ C/W = 117.2^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 32-PIN LQFP, FORCED CONVECTION**

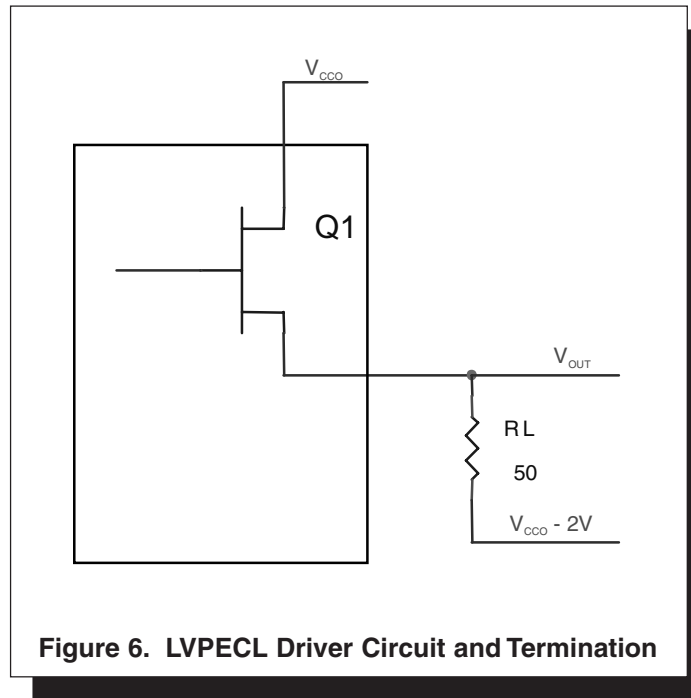
| <b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b> |          |            |            |
|--|----------|------------|------------|
|  | <b>0</b> | <b>200</b> | <b>500</b> |
| Single-Layer PCB, JEDEC Standard Test Boards                         | 67.8°C/W | 55.9°C/W   | 50.1°C/W   |
| Multi-Layer PCB, JEDEC Standard Test Boards                          | 47.9°C/W | 42.1°C/W   | 39.4°C/W   |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 6.



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.935V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.67V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.67V$$

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 30.94mW$



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|--|----------|----------|----------|
|  | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS85310I-31 is: 1216



PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

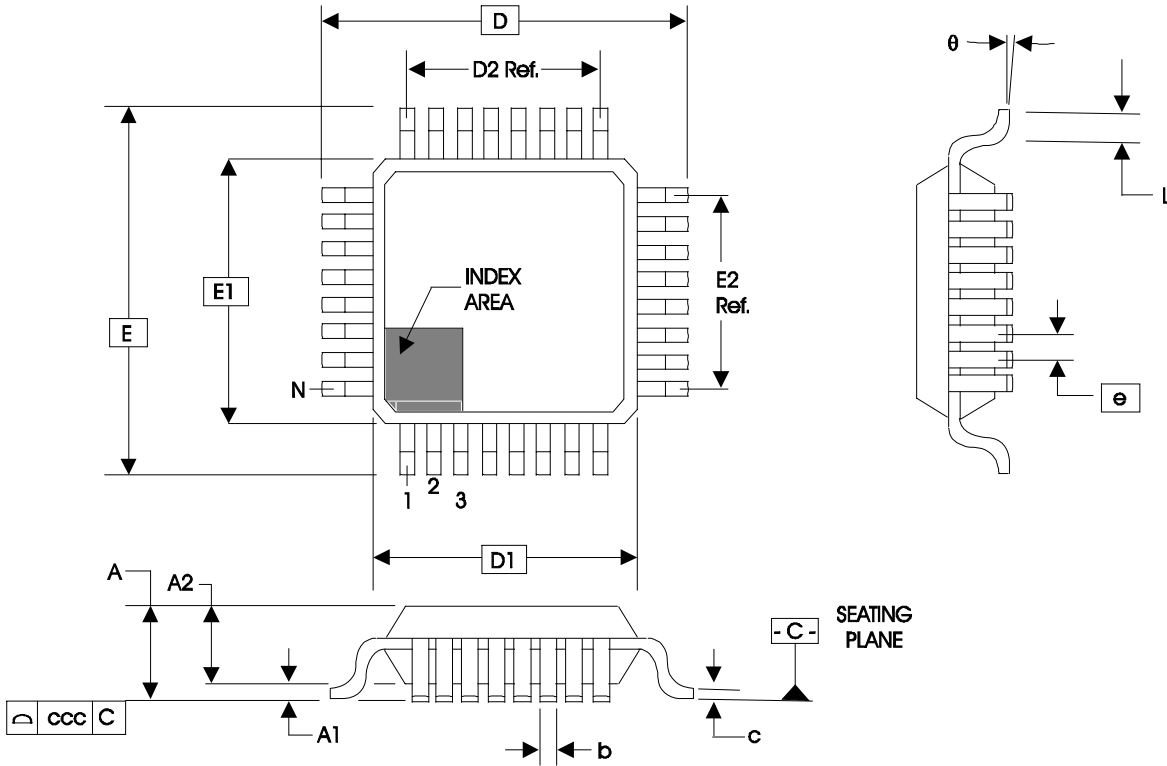


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--|------------|---------|---------|
| SYMBOL   | BBA        |         |         |
|  | MINIMUM    | NOMINAL | MAXIMUM |
| N  | 32         |         |         |
| A  | --         | --      | 1.60    |
| A1   | 0.05       | --      | 0.15    |
| A2   | 1.35       | 1.40    | 1.45    |
| b  | 0.30       | 0.37    | 0.45    |
| c  | 0.09       | --      | 0.20    |
| D  | 9.00 BASIC |         |         |
| D1   | 7.00 BASIC |         |         |
| D2   | 5.60 Ref.  |         |         |
| E  | 9.00 BASIC |         |         |
| E1   | 7.00 BASIC |         |         |
| E2   | 5.60 Ref.  |         |         |
| e  | 0.80 BASIC |         |         |
| L  | 0.45       | 0.60    | 0.75    |
| theta  | 0°         | --      | 7°      |
| ccc  | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

# ICS85310I-31

## LOW SKEW, DUAL, 1-TO-5 2.5V/3.3V DIFFERENTIAL-TO-ECL/LVPECL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking       | Package                  | Shipping Packaging | Temperature   |
|-------------------|---------------|--------------------------|--------------------|---------------|
| ICS85310AYI-31    | ICS85310AYI31 | 32 lead LQFP             | tray               | -40°C to 85°C |
| ICS85310AYI-31T   | ICS85310AYI31 | 32 lead LQFP             | 1000 tape & reel   | -40°C to 85°C |
| ICS85310AYI-31LF  | ICS5310AI31L  | 32 lead "Lead Free" LQFP | tray               | -40°C to 85°C |
| ICS85310AYI-31LFT | ICS5310AI31L  | 32 lead "Lead Free" LQFP | 1000 tape & reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

The aforementioned trademark, HiPerClockS is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries. While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.



| REVISION HISTORY SHEET |       |         |  |          |
|------------------------|-------|---------|--|----------|
| Rev                    | Table | Page    | Description of Change  | Date     |
| A                      |       | 9       | Added Termination for LVPECL Outputs.  | 5/30/02  |
| A                      |       |         | Updated part number from ICS85310-31 to ICS85310I-31 throughout the data sheet to reflect operating temperature. | 7/24/02  |
| A                      | T9    | 14      | Corrected Marking from ICS85310AYI-31 to ICS85310AYI31.  | 7/25/02  |
| B                      | T4A   | 4       | Power Supply table - increased max. value for $I_{EE}$ to 120mA from 30mA max.                                   | 10/23/02 |
|                        |       | 10      | Power Considerations have re-adjusted to the increased $I_{EE}$ value.   |          |
| C                      | T2    | 2       | Pin Characteristics Table - changed 4pF max. to 4pF typical.   | 7/31/03  |
|                        |       | 4       | Updated Absolute Maximum Ratings.  |          |
|                        | T4D   | 5       | LVPECL DC Characteristics Table - changed $V_{SWING}$ from 0.85V max. to 1.0V max.                               |          |
|                        |       | 8 & 9   | Application section added, <i>Termination for 2.5V LVPECL Outputs and Differential Clock Input Interface.</i>    |          |
|                        |       | 10 & 11 | Power Considerations - recalculated Total Power Dissipation for 3.8V.  |          |
|                        |       | 14      | Ordering Information Table - corrected marking from ICS85310AYI31 to ICS85310AI-31.                              |          |
| D                      |       | 1       | Features Section - added Additive Phase Jitter bullet and Lead-Free bullet.                                      | 7/6/05   |
|                        | T5    | 5       | AC Characteristics Table - added Additive Phase Jitter row.  |          |
|                        |       | 6       | Added Additive Phase Jitter Section.   |          |
|                        | T9    | 14      | Ordering Information Table - added Lead-Free Part Number and Note.   |          |